CERTIFICATE

I, Takumi SASAKI, residing at 1-11-11, Higashi-oowada, Ichikawa-shi, Chiba-ken, 272-0026 Japan, hereby certify that I am the translator of the attached document, namely a Certified Copy of Japanese Patent Application No. 2000-003942 and certify that the following is a true translation to the best of my knowledge and belief.

Takumi Sasaki July 25, 2003

Signature of Translator Date

[Name of Document] SPECIFICATION

[Title of the Invention] METHOD FOR MANUFACTURING CONNECTION BOARD, CONNECTION BOARD, METHOD FOR MANUFACTURING SEMICONDUCTOR DEVICE, AND SEMICONDUCTOR DEVICE

[Claims]

[Claim 1] A method for manufacturing a connection board, comprising the steps of forming metal wiring lines on a substrate, providing an insulating agent over the metal wiring lines to form a flexible insulating layer, forming another metal wiring lines on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, and separating the metal wiring lines and the insulating layer from the substrate.

[Claim 2] The connection board-manufacturing method according to Claim 1, wherein the metal wiring lines and the insulating layer form a multilayer structure.

[Claim 3] The connection board-manufacturing method according to Claim 1 or 2, wherein the substrate comprises glass.

[Claim 4] A connection board manufactured by a connection board-manufacturing method according to any one of Claims 1 to 3.

[Claim 5] A method for manufacturing a semiconductor device, comprising the steps of forming metal wiring lines on a substrate; providing an insulating agent over the metal wiring lines to form a flexible insulating layer; forming another metal wiring lines on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, whereby a connection board is formed on the substrate; connecting semiconductor chips to the metal wiring lines disposed on the upper surface of the connection board; and separating the connection board from the substrate.

[Claim 6] A method for manufacturing a semiconductor device, comprising the steps of forming metal wiring lines, connected to elements arranged on semiconductor chips with butt joints, on a first substrate; providing an insulating agent over the metal wiring lines to form a flexible insulating layer; forming another metal wiring lines on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, whereby a connection board is formed on the substrate; causing a second substrate to adhere to the upper surface of the connection board; transferring the connection board from the first substrate to the second substrate;

connecting the semiconductor chips to the metal wiring lines separated from the surface of the first substrate; and separating the connection board from the second substrate.

[Claim 7] The semiconductor device-manufacturing method according to Claim 5 or 6, wherein a plurality of the semiconductor chips are mounted on the connection board.

[Claim 8] The semiconductor device-manufacturing method according to Claim 5 or 6, wherein the metal wiring lines and the insulating layer form a multilayer structure.

[Claim 9] The semiconductor device-manufacturing method according to Claim 5, wherein the substrate comprises glass.

[Claim 10] The semiconductor device-manufacturing method according to Claim 5, wherein the substrate comprises silicon.

[Claim 11] The semiconductor device-manufacturing method according to Claim 6, wherein the second substrate comprises glass.

[Claim 12] The semiconductor device-manufacturing method according to Claim 6, wherein the second substrate comprises silicon.

[Claim 13] A semiconductor device manufactured by a semiconductor device-manufacturing method according to any one of Claims 5 to 12.

[Detailed Description of the Invention]

[0001]

[Technical Field of the Invention]

The present invention relates to connection boards, methods for manufacturing such connection boards, semiconductor devices, and methods for manufacturing such semiconductor devices. The present invention particularly relates to a connection board including a flexible insulating material, a method for manufacturing such a connection board, a semiconductor device, and a method for manufacturing such a semiconductor device.

[0002]

[Description of the Related Art]

Conventionally, a connection board included in a multiple chip package (hereinafter referred to as "MCP") manufactured according to the following procedure has been known: a wiring pattern is formed on an insulating film (usually a polyimide film) and a plurality of semiconductor chips are mounted on the wiring pattern.

[0003]

In the MCP having the above configuration, in order to reduce the volume thereof, the insulating film is folded (so as to avoid the semiconductor chips), that is, the MCP is folded. Furthermore, the MCP can be connected to another board with connection electrodes disposed on the back surface of the insulating film, the back surface being opposite to a surface on which the semiconductor chips

arranged.

[0004]

In the above connection board, copper foil for forming a wiring pattern is joined to the flexible insulating film, a resist material is provided on the copper foil, and a wiring pattern is formed by performing the exposure and etching of the resulting film.

[0005]

[Problems to be Solved by the Invention]

In the connection board and a semiconductor device including the connection board, there are the following problems.

[0006]

For the connection board, since the insulating film is flexible, the insulating film is readily deformed by external forces and its own weight. Therefore, the insulating film cannot be readily rendered flat in an exposure step. Thus, it is difficult to reduce the pitch of the wiring pattern and the pitch between wiring patterns (from the viewpoint of focusing).

[0007]

In order to cope with complicated wiring lines arranged between semiconductor chips, the following technique has been known: wiring patterns are each formed on a plurality of corresponding layers. However, there is a problem in

that it is difficult to form such wiring patterns on corresponding layers from the viewpoint of structure because the patterns are formed on the insulating film.

[0008]

Since the insulating film has a thickness of about 50 μm, a large force is necessary to fold the insulating film. Therefore, if the folding force is insufficient, there is a fear that the folded insulating film expands due to the restoring force thereof (the folded insulating film is restored to the original state).

[0009]

In the semiconductor device, semiconductor chips are usually joined to a wiring pattern arranged on the connection board by a thermocompression bonding process using a heating tool when the semiconductor chips are mounted on the connection board. Since the semiconductor chips comprising monocrystalline silicon are greatly different in thermal expansion coefficient from the connection board comprising a polyimide material, there is a problem in that it is difficult to reduce the pattern pitch.

[0010]

Furthermore, in the semiconductor device, the connection board is readily deformed by external forces because the connection board remains flexible after the semiconductor chips are mounted thereon. Thus, there is a

fear that wiring lines are broken when external forces are applied to the connection board and therefore stresses arise between the semiconductor chips and the connection board.

[0011]

In order to solve the above conventional problems, it is an object of the present invention to provide a connection board, a method for manufacturing such a connection board, a semiconductor device, and a method for manufacturing such a semiconductor device. In the connection board, the width and pitch of the wiring lines can be reduced, a multi-level interconnect structure can be formed, and defects, such as breaks in the wiring lines, due to external forces can be prevented.

[0012]

[Means for Solving the Problems]

A method for manufacturing a connection board according to Claim 1 includes the steps of forming metal wiring lines on a substrate, providing an insulating agent over the metal wiring lines to form a flexible insulating layer, forming another metal wiring lines on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, and separating the metal wiring lines and the insulating layer from the substrate. According to the connection board set forth in

Claim 1, since the substrate is not flexible, deformation is not caused on the surface by external forces or its own weight. Therefore, in a step of forming the metal lines, for example, in an exposure sub-step, the substrate is not moved in the direction of the depth of field. Thus, precise exposure can be performed and therefore the metal wiring lines having a small width and pitch can be formed.

[0013]

Furthermore, since the insulating agent is provided on the substrate such that the insulating agent covers the metal wiring lines, the thickness of the insulating layer can be set to such a value that is sufficient for the insulating layer to cover the metal wiring lines. Thus, the insulating layer may have a small thickness and therefore the connection board can be folded by a small force. Furthermore, since the insulating layer has a small restoring force (spring back force), the folded connection board can be prevented from being expanded (the folded insulating film is prevented from being restored to the original state).

[0014]

In the connection board-manufacturing method according to Claim 2, the metal wiring lines and the insulating layer form a multilayer structure. According to the connection board-manufacturing method set forth in Claim 2, the metal

wiring lines disposed on and under the insulating layer can be connected to each other with contact holes extending through the insulating layer. Therefore, the wiring lines can be prevented from interfering each other even if the number of the wiring lines is increased. Thus, the wiring lines can be readily arranged in the connection board.

[0015]

In the connection board-manufacturing method according to Claim 3, the substrate comprises glass. According to the connection board-manufacturing method set forth in Claim 3, light can be applied to the connection board through the back surface (a surface opposite to one on which the connection board is placed) of the glass substrate. Thus, if a solvent or the like having a release function provided by the application of light is placed between the glass substrate and the connection board, the connection board can be readily separated from the glass substrate by applying light to the back surface of the glass substrate after the formation of the connection board.

[0016]

A connection board according to Claim 4 is manufactured by a connection board-manufacturing method set forth in any one of Claims 1 to 3. According to the connection board set forth in Claim 4, the metal wiring lines having a small width and pitch can be formed.

[0017]

A method for manufacturing a semiconductor device according to Claim 5 includes the steps of forming metal wiring lines on a substrate; providing an insulating agent over the metal wiring lines to form a flexible insulating layer; forming another metal wiring lines on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, whereby a connection board is formed on the substrate; connecting semiconductor chips to the metal wiring lines disposed on the upper surface of the connection board; and separating the connection board from the substrate. According to the semiconductor device-manufacturing method set forth in Claim 5, since the substrate is not flexible, deformation is not caused on the surface by external forces or its own weight. Therefore, in a step of forming the metal lines, for example, in an exposure sub-step, the substrate is not moved in the direction of the depth of field. Thus, precise exposure can be performed and therefore the metal wiring lines having a small width and pitch can be formed.

[0018]

Furthermore, since the insulating agent is provided on the substrate such that the insulating agent covers the

metal wiring lines, the thickness of the insulating layer can be set to such a value that is sufficient for the insulating layer to cover the metal wiring lines. Thus, the insulating layer may have a small thickness and therefore the connection board can be folded by a small force. Furthermore, since the insulating layer has a small restoring force (spring back force), the folded connection board can be prevented from being expanded (the folded insulating film is prevented from being restored to the original state).

[0019]

In addition to the above advantages, terminals of the semiconductor chips are not isolated when the semiconductor chips are mounted on the connection board, because the connection board is placed on the non-flexible, flat substrate. Thus, electrical discontinuity can be prevented from being caused between the semiconductor chip terminals and the metal wiring lines. If the substrate comprises a material having a thermal expansion coefficient close to that of the semiconductor chips, short circuits can be prevented from being caused between the terminals adjacent to each other, wherein such short circuits are due to an increase in difference in expansion between each metal wiring line and semiconductor chip to which radiant heat emitted from a heating tool is applied during the mounting

of the semiconductor chips.

[0020]

The semiconductor device is separated from the substrate after the mounting of the semiconductor chips in the final step. Thus, in processing steps including a transporting step, since the substrate supports the semiconductor device, deformation caused in the semiconductor device by external forces can be prevented.

[0021]

A method for manufacturing a semiconductor device according to Claim 6 includes the steps of forming metal wiring lines, connected to elements arranged on semiconductor chips with butt joints, on a first substrate; providing an insulating agent over the metal wiring lines to form a flexible insulating layer; forming another metal wiring lines on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, whereby a connection board is formed on the substrate; causing a second substrate to adhere to the upper surface of the connection board; transferring the connection board from the first substrate to the second substrate; connecting the semiconductor chips to the metal wiring lines separated from the surface of the first substrate; and separating the connection board from

the second substrate. According to the semiconductor device-manufacturing method set forth in Claim 6, since the first substrate is not flexible, deformation is not caused on the surface by external forces or its own weight. Therefore, in a step of forming the metal lines, for example, in an exposure sub-step, the substrate is not moved in the direction of the depth of field. Thus, precise exposure can be performed and therefore the metal wiring lines having a small width and pitch can be formed.

[0022]

Furthermore, since the insulating agent is provided on the substrate such that the insulating agent covers the metal wiring lines, the thickness of the insulating layer can be set to such a value that is sufficient for the insulating layer to cover the metal wiring line. Thus, the insulating layer may have a small thickness and therefore the connection board can be folded by a small force. Furthermore, since the insulating layer has a small restoring force (spring back force), the folded connection board can be prevented from being expanded (the folded insulating film is prevented from being restored to the original state).

[0023]

Since the connection board is formed on the first substrate and the resulting connection board is then

transferred to the second substrate, a surface of the connection board separated from the first substrate is exposed after the connection board is transferred to the second substrate. The metal wiring lines to be connected to elements arranged on semiconductor chips with butt joints are disposed on the exposed surface separated from the first substrate. Thus, the semiconductor chips can be electrically connected to the connection board if other metal wiring lines are not arranged on a surface on which the semiconductor chips are placed.

[0024]

Furthermore, terminals of the semiconductor chips are not isolated when the semiconductor chips are mounted on the connection board, because the connection board is placed on the non-flexible, flat substrate. Thus, electrical discontinuity can be prevented from being caused between the semiconductor chip terminals and the metal wiring lines. If the substrate comprises a material having a thermal expansion coefficient close to that of the semiconductor chips, short circuits can be prevented from being caused between the terminals adjacent to each other, wherein such short circuits are due to an increase in difference in expansion between each metal wiring line and semiconductor chip to which radiant heat emitted from a heating tool is applied during the mounting of the semiconductor chips.

[0025]

The semiconductor device is separated from the second substrate after the mounting of the semiconductor chips in the final step. Thus, in processing steps including a transporting step, since the first substrate supports the connection board and the second substrate supports the semiconductor device, deformation caused in the semiconductor device by external forces can be prevented.

[0026]

In the semiconductor device-manufacturing method according to Claim 7, a plurality of the semiconductor chips are mounted on the connection board. According to the semiconductor device-manufacturing method set forth in Claim 7, a plurality of the semiconductor chips can be connected to each other by mounting the semiconductor chips on the connection board, thereby achieving multifunctional devices. Since the insulating layer is flexible, the connection board can be folded along each line between the semiconductor chips, thereby reducing the volume of the semiconductor device.

[0027]

In the semiconductor device-manufacturing method according to Claim 8, the metal wiring lines and the insulating layer form a multilayer structure. According to the semiconductor device-manufacturing method set forth in

Claim 8, the metal wiring lines disposed on and under the insulating layer can be connected to each other with contact holes extending through the insulating layer. Therefore, the metal wiring lines can be prevented from interfering each other even if the number of the metal wiring lines is increased. Thus, the metal wiring lines can be readily arranged in the connection board.

[0028]

In the semiconductor device-manufacturing method according to Claim 9, the substrate comprises glass. According to the semiconductor device-manufacturing method set forth in Claim 9, light can be applied to the connection board through the back surface (a surface opposite to one on which the connection board is placed) of the glass substrate. Thus, if a solvent or the like having a release function provided by the application of light is placed between the glass substrate and the connection board, the connection board can be readily separated from the glass substrate by applying light to the back surface of the glass substrate after the formation of the connection board.

[0029]

In the semiconductor device-manufacturing method according to Claim 10, the substrate comprises silicon. According to the semiconductor device-manufacturing method set forth in Claim 10, the connection board is tightly in

contact with the silicon substrate in a step of mounting the semiconductor chips on the connection board. Since the substrate has substantially the same thermal expansion coefficient as that of the semiconductor chips, short circuits can be prevented from being caused between the terminals adjacent to each other, wherein such short circuits are due to an increase in difference in expansion between each metal wiring line and semiconductor chip to which radiant heat emitted from a heating tool used for the mounting of the semiconductor chips is applied.

[0030]

In the semiconductor device-manufacturing method according to Claim 11, the second substrate comprises glass. According to the semiconductor device-manufacturing method set forth in Claim 11, light can be applied to the connection board through the back surface (a surface opposite to one having the connection board thereon) of the glass substrate. Thus, if a solvent or the like having a release function provided by the application of light is placed between the glass substrate and the connection board, the connection board can be readily separated from the glass substrate by applying light to the back surface of the glass substrate after the formation of the connection board.

[0031]

In the semiconductor device-manufacturing method

according to Claim 12, the second substrate comprises silicon. According to the semiconductor device-manufacturing method set forth in Claim 12, the connection board is tightly in contact with the silicon substrate in a step of mounting the semiconductor chips on the connection board. Since the substrate has substantially the same thermal expansion coefficient as that of the semiconductor chips, short circuits can be prevented from being caused between the terminals adjacent to each other, wherein such short circuits are due to an increase in difference in expansion between each metal wiring line and semiconductor chip to which radiant heat emitted from a heating tool used for the mounting of the semiconductor chips is applied.

[0032]

A semiconductor device according to Claim 13 is manufactured by a semiconductor device-manufacturing method according to any one of Claims 5 to 12. According to the semiconductor device set forth in Claim 13, since the insulating layer is flexible and has a small thickness, the connection board can be readily folded. Furthermore, since the insulating layer has a small restoring force (spring back force), the folded connection board can be prevented from being expanded (the folded insulating film is prevented from being restored to the original state).

[0033]

[Description of the Embodiments]

For a connection board, method for manufacturing such a connection board, semiconductor device, and method for manufacturing such a semiconductor device according to the present invention, the preferred embodiments will now be described in detail with reference to the accompanying drawings.

[0034]

FIG. 1 includes a perspective view and side elevational view showing a configuration of a semiconductor device according to this embodiment. FIG. 2 includes an enlarged sectional view and rear elevational view showing a principal part of a configuration of the semiconductor device.

[0035]

As shown in these figures, the semiconductor device 10 according to this embodiment (herein referred to as "semiconductor device 10") includes a flexible connection board 12 and a plurality of semiconductor chips 14 (three semiconductor chips are used in this embodiment) arranged on one surface of the connection board 12.

[0036]

The connection board 12, which is a component of the semiconductor device 10, is a strip having a constant width and has a surface 13 on which first metal wiring lines 16 for providing electrical connections to the semiconductor

chips 14 are arranged. The first metal wiring lines 16 arranged on the surface 13 each extend to a back surface 20 of the connection board 12 through corresponding contact holes 18 and are connected to corresponding second metal wiring lines 22 arranged on the back surface (see FIG. 2(2)). Soldering balls 26 are each placed on corresponding connector lands 24 arranged on the second metal wiring lines 22 such that the connection board 12 can be connected to an external board, which is not shown, with the soldering balls 26.

[0037]

Since the connection board 12 is flexible, after the semiconductor chips 14 are mounted on the connection board 12 as shown in FIG. 1(1), the connection board 12 can be folded along folding lines 27 set between the semiconductor chips 14, as shown in FIG. 1(2), thereby reducing the surface mounting area of the semiconductor device 10.

[0038]

As shown in FIG. 2(2), a large number of the connector lands 24 are arranged at an end portion of a surface of the connection board 12, and the second metal wiring lines 22 each extending through the corresponding contact holes 18 are each connected to the corresponding predetermined connector lands 24 in such a manner that the second metal wiring lines 22 extend between other contact holes 18.

[0039]

A method for manufacturing the semiconductor device 10 having the above configuration will now be described.

[0040]

FIGS. 3 to 5 are illustrations showing steps of manufacturing the semiconductor device 10. As shown in FIG. 3(1), a first glass substrate 28 functioning as a non-flexible substrate or a first non-flexible substrate is prepared. As shown in FIG. 3(2), the first glass substrate 28 is placed in an argon atmosphere having a pressure of 2-5 mTorr and a temperature of 150-300°C and sputtering is then performed with an input DC electric power of 9-12 kW using a target containing Al-Cu, Al-Si-Cu, Al-Si, Ni, Cr, Au, or the like, thereby forming a metal layer 30, having the same composition as that of the target and a thickness of 200-20000 angstroms, for forming the first metal wiring lines 16. Alternatively, the metal layer 30 may be formed according to the following procedure other than the above procedure: an Au layer having a thickness of about 1000 angstroms is formed on a Cr base layer by deposition.

[0041]

After the metal layer 30 is formed on the first glass substrate 28 as described above, a photoresist layer, which is not shown, is formed on the metal layer 30. The photoresist layer is patterned by a photolithographic

process, portions of the photoresist layer other than regions for forming the first metal wiring lines 16 are removed, and the metal layer 30 is then etched using the resulting photoresist layer as a mask. FIG. 3(3) shows the arrangement of the first metal wiring lines 16 formed by etching the metal layer 30.

[0042]

The pattern of the first metal wiring lines 16 is formed such that the first metal wiring lines 16 are directly connected to terminals of elements such as transistors, resistors, and capacitors with butt joints. Therefore, the first metal wiring lines 16 are electrically connected to the semiconductor chips 14 when their surfaces are joined to each other.

[0043]

After the first metal wiring lines 16 are formed on the first glass substrate 28 as described above, a polyimide material functioning as an insulating material is provided over the first metal wiring lines 16 such that the first metal wiring lines 16 is covered with the polyimide material. The polyimide material is then cured, thereby forming an insulating layer 32. This situation is shown in FIG. 3(4). Since the raw material of the insulating layer 32 includes the polyimide material, the insulating layer 32 is flexible after the curing. Therefore, the first metal wiring lines

16 and the insulating layer 32 are deformed by external forces and their own weight after the first metal wiring lines 16 and the insulating layer 32 are separated from the first glass substrate 28.

[0044]

After the insulating layer 32 is formed so as to cover the first metal wiring lines 16, another photoresist layer, which is not shown, is formed on the insulating layer 32. The photoresist layer is patterned by a photolithographic process, regions for forming the contact holes 18 are removed, and the insulating layer 32 is then etched using the resulting photoresist layer as a mask, thereby allowing the first metal wiring lines 16 to be each exposed at the bottoms of the corresponding contact holes 18.
FIG. 4(1) shows the arrangement of the contact holes 18 formed by etching the insulating layer 32.

[0045]

After the contact holes 18 are formed as described above, another metal layer 34 is formed such that the contact holes 18 are filled with portions of the metal layer 34 and the insulating layer 32 is covered with the metal layer 34, as shown in FIG. 4(2). The metal layer 34 is formed in the same manner as that in the metal layer 30. That is, the resulting first glass substrate 28 is placed in an argon atmosphere having a pressure of 2-5 mTorr and a

temperature of 150-300°C and sputtering is then performed with an input DC electric power of 9-12 kW using a target containing Al-Cu, Al-Si-Cu, Al-Si, Ni, Cr, Au, or the like, thereby forming the metal layer 34, having the same composition as that of the target and a thickness of 200-20000 angstroms, for forming the second metal wiring lines 22.

[0046]

After the metal layer 34 is formed on the insulating layer 32, another photoresist layer, which is not shown, is formed on the metal layer 34. The photoresist layer is patterned by a photolithographic process, portions of the photoresist layer other than regions for forming the second metal wiring lines 22 are removed, and the metal layer 34 is then etched using the resulting photoresist layer as a mask. FIG. 4(3) shows the arrangement of the second metal wiring lines 22 formed by etching the metal layer 34. Since the second metal wiring lines 22 are each disposed on the corresponding contact holes 18, the second metal wiring lines 22 are each electrically connected to the corresponding first metal wiring lines 16 with the corresponding contact holes 18. Thus, the first metal wiring lines 16 and the second metal wiring lines 22 are each arranged on corresponding surfaces of the insulating layer 32, thereby obtaining the flexible connection board 12

disposed on the first glass substrate 28. In the connection board 12 having the above configuration, the metal wiring lines are formed on and above the first glass substrate 28, which is not flexible. That is, the first glass substrate 28 is not deformed by external forces and its own weight. Therefore, when the photoresist layers are each provided on the metal layer 30 and the metal layer 34, correct focus can be achieved, whereby the wiring lines having a small width and pitch can be formed. Thus, as shown in FIG. 2(2), the following wiring routes can be obtained: a plurality of the second metal wiring lines 22 extend between the connector lands 24 arranged in matrix and are connected to the arbitrary connector lands 24.

[0047]

After the connection board 12 is formed as described above, a second glass substrate 36 similar to the first glass substrate 28 is placed on the connection board 12, thereby causing the second glass substrate 36 to adhere to a surface of the connection board 12 on which the second metal lines 22 are arranged. This situation is shown in FIG. 4(4). After the second glass substrate 36 is caused to adhere to the surface of the connection board 12 on which the second metal lines 22 are arranged, the second glass substrate 36 is lifted up, thereby transferring the connection board 12 from the first glass substrate 28 to the second glass

substrate 36. This situation is shown in FIG. 5(1). In this transfer operation, if a solvent or the like having a release function provided by the application of light is placed between the first glass substrate 28 and the connection board 12 in advance by applying such a solvent onto the first glass substrate 28, the connection board 12 can be readily separated from the first glass substrate 28 by applying light to the back surface of the first glass substrate 28 after the formation of the connection board 12. Alternatively, the procedure below may be performed. An adhesive having adhesion that is lowered by the application of ultraviolet rays or X-rays is applied onto the first glass substrate 28 in advance, and the connection board 12 is then formed on the adhesive layer. In a step of separating the connection board 12 from the first glass substrate 28, ultraviolet rays or X-rays are applied to the back surface of the first glass substrate 28 such that the adhesion of the adhesive disposed on the first glass substrate 28 is lowered, thereby separating the connection board 12 from the first glass substrate 28.

[0048]

As shown in FIG. 5(2), after the connection board 12 is transferred from the first glass substrate 28 to the second glass substrate 36, the second glass substrate 36 is moved to a location above a mounting stage 38 having the

semiconductor chips 14 thereon. As shown in FIG. 5(3), the first metal wiring lines 16 are each joined to corresponding terminal portions 40 of elements disposed on the semiconductor chips 14 by a thermocompression bonding process. If the second glass substrate 36 comprises a material having a thermal expansion coefficient close to that of monocrystalline silicon for forming base plates of the semiconductor chips 14, the pitch deviation can be allowed to remain small when the connection board 12 and the second glass substrate 36, which are tightly in contact with each other, are heated by radiant heat emitted from a tool for the thermocompression bonding, wherein the pitch deviation is due to the difference between the thermal expansion coefficients. If a substrate comprising monocrystalline silicon is used instead of the second glass substrate 36, the pitch deviation due to an increase in temperature can be minimized because such a substrate has the same thermal expansion coefficient as that of the semiconductor chips 14. Since the connection board 12 is tightly in contact with the second glass substrate 36, the connection board 12 does not expand in the thickness direction while the semiconductor chips 14 are mounted to the connection board 12. Thus, the semiconductor chips 14 can be securely mounted to the connection board 12 without causing short circuits.

[0049]

After the semiconductor chips 14 are mounted to the connection board 12, the connection board 12 is transported together with the second glass substrate 36 without separating the connection board 12 from the second glass substrate 36 until the final processing step. Since the connection board 12 is tightly in contact with the second glass substrate 36 during the transportation, the deformation of the semiconductor device 10 caused by the own weight of the semiconductor device 10 or external forces applied to the semiconductor device 10 can be prevented during the transportation. Thereby, the following problems can be prevented in advance: the buckling and deformation of the connection board 12 and the separation of the semiconductor chips 14 from the connection board 12.

[0050]

As shown in FIG. 5(4), in the final step, the semiconductor device 10 is separated from the second glass substrate 36 (the separation procedure is the same as that for the first glass substrate 28), and the resulting semiconductor device 10 is then folded along the folding lines 27. Since the insulating layer 32 has such a thickness that is enough to cover the first metal wiring lines 16 having a thickness of 5-10 μm, a thickness of 10-20 μm is sufficient for the insulating layer 32. Therefore,

the semiconductor device 10 can be more readily folded as compared with one including a conventional insulating film (the thickness is about 50 μm) and it can be prevented that the folded insulating layer 32 is expanded by the restoring force thereof.

[0051]

In this embodiment, the semiconductor chips 14 are connected to the first metal wiring lines 16 is separated from the first glass substrate 28. However, the present invention is not limited to this embodiment and the semiconductor chips may be mounted on a surface having the second metal wiring lines 22 thereon. In this case, the semiconductor chips are mounted on both one surface having the first metal wiring lines 16 thereon and the other surface having the second metal wiring lines 22 thereon, thereby enhancing the function of the semiconductor device 10.

[0052]

In this embodiment, the connection board 12 has a double-layer structure. However, the present invention is not limited to this embodiment and the connection board 12 may have a multi-level interconnect structure having a plurality of wiring lines and insulating layers. When the connection board 12 has such a multi-level interconnect structure, the wiring lines can be prevented from

interfering each other by arranging the wiring lines on different layers even if the number of the wiring lines is increased due to an increase in number of semiconductor chip pins or an increase in number of mounted semiconductor chips. Thus, the wiring lines can be readily arranged in the connection board.

[0053]

[Advantages]

As described above, according to the connection board-manufacturing method set forth in Claim 1, metal wiring lines are formed on a substrate, an insulating agent is provided over the metal wiring lines such that a flexible insulating layer is formed, another metal wiring lines are formed on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, and the metal wiring lines and the insulating layer are separated from the substrate; hence, the width and pitch of the wiring lines can be reduced and a multi-level interconnect structure can be obtained.

[0054]

According to the connection board set forth in Claim 4, the connection board is manufactured by a connection board-manufacturing method of any one of Claims 1 to 3; hence, the

width and pitch of the wiring lines can be reduced and a multi-level interconnect structure can be obtained.

[0055]

Furthermore, according to the semiconductor device-manufacturing method set forth in Claim 5, metal wiring lines are formed on a substrate; an insulating agent is provided over the metal wiring lines such that a flexible insulating layer is formed; another metal wiring lines are formed on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, whereby a connection board is formed on the substrate; semiconductor chips are connected to the metal wiring lines disposed on the upper surface of the connection board; and the connection board is then separated from the substrate. Thus, the width and pitch of the wiring lines can be reduced, a multi-level interconnect structure can be obtained, problems due to radiant heat emitted from a heating tool or the like can be reduced during the mounting of the semiconductor chips, and problems such as line breaks caused by external forces can be prevented.

[0056]

According to the semiconductor device-manufacturing method set forth in Claim 6, metal wiring lines connected to

elements, arranged on semiconductor chips, with butt joints are formed on a first substrate; an insulating agent is provided over the metal wiring lines such that a flexible insulating layer is formed; another metal wiring lines are formed on the insulating layer such that the metal wiring lines disposed on and under the insulating layer are electrically connected to each other with contact holes extending in the insulating layer, whereby a connection board is formed on the substrate; a second substrate is caused to adhere to the upper surface of the connection board; the connection board is transferred from the first substrate to the second substrate; the semiconductor chips are connected to the metal wiring lines separated from the surface of the first substrate; and the connection board is then separated from the second substrate. Thus, the width and pitch of the wiring lines can be reduced and a multi-level interconnect structure can be obtained. Furthermore, the semiconductor chips can be electrically connected to the connection board with butt joints even if the semiconductor chips do not have wiring lines thereon. Problems due to radiant heat emitted from a heating tool or the like can be reduced during the mounting of the semiconductor chips, and problems such as line breaks caused by external forces can be prevented.

[0057]

According to the semiconductor device set forth in Claim 13, since the semiconductor device is manufactured by a semiconductor device-manufacturing method according to any one of Claims 5 to 12, the insulating layer has a small thickness. Therefore, the semiconductor device can be readily folded. Furthermore, the folded semiconductor device can be prevented from being expanded.

[Brief Description of the Drawings]

[FIG. 1]

FIG. 1 includes a perspective view and side elevational view showing a configuration of a semiconductor device according to this embodiment.

[FIG. 2]

FIG. 2 includes an enlarged sectional view and rear elevational view showing a principal part of a configuration of the semiconductor device.

[FIG. 3]

FIG. 3 is an illustration showing steps of manufacturing a semiconductor device 10.

[FIG. 4]

FIG. 4 is an illustration showing steps of manufacturing the semiconductor device 10.

[FIG. 5]

FIG. 5 is an illustration showing steps of manufacturing the semiconductor device 10.

[Reference Numerals]

10: semiconductor device

12: connection board

13: surface

14: semiconductor chips

16: first metal wiring lines

18: contact holes

20: back surface

22: second metal wiring lines

24: connector lands

26: soldering balls

27: folding lines

28: first glass substrate

30: metal layer

32: insulating layer

34: metal layer

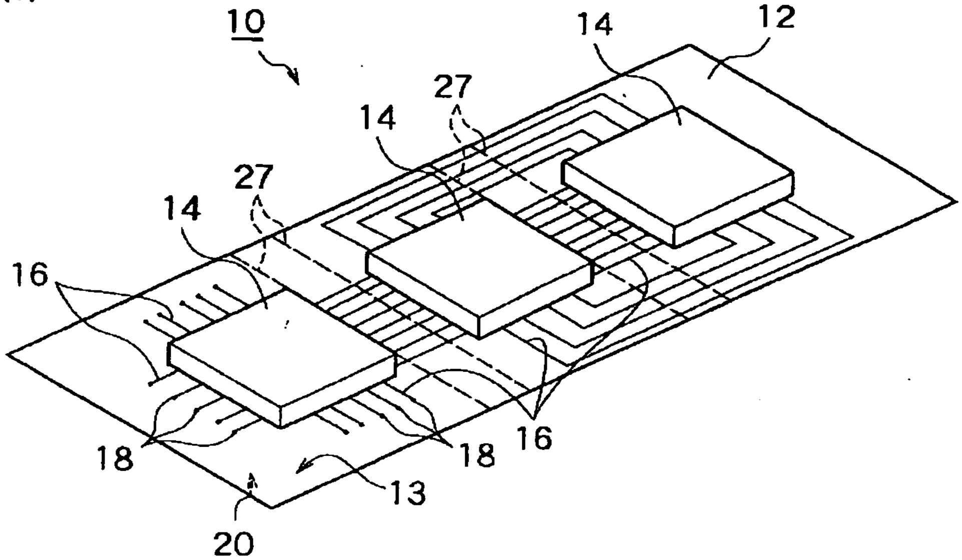
36: second glass substrate

38: mounting stage

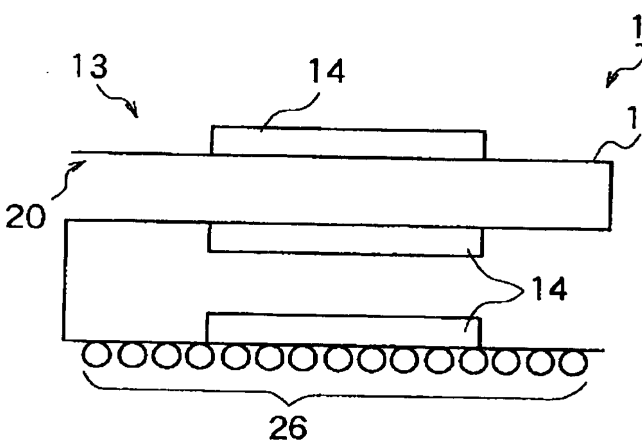
40: terminal portions

FIG.1

(1)



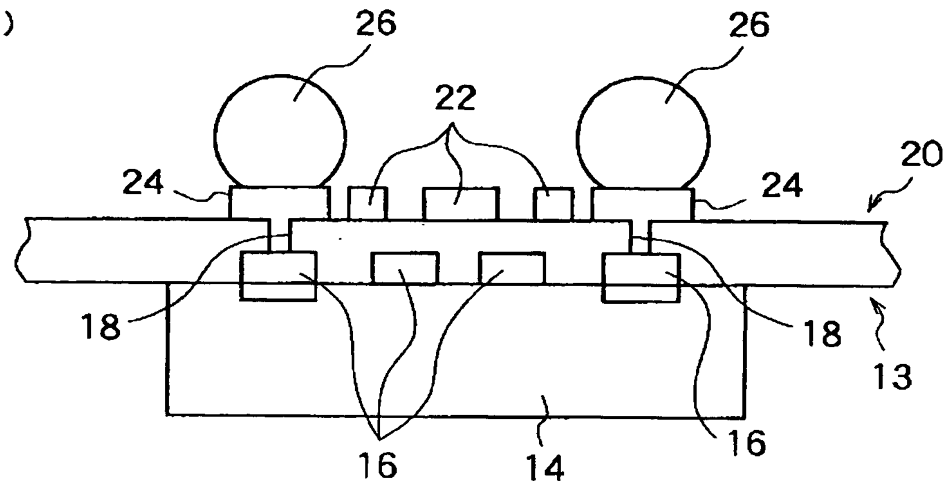
(2)



10: SEMICONDUCTOR DEVICE
12: CONNECTION BOARD
14: SEMICONDUCTOR CHIPS
16: FIRST METAL WIRING LINES

FIG.2

(1)



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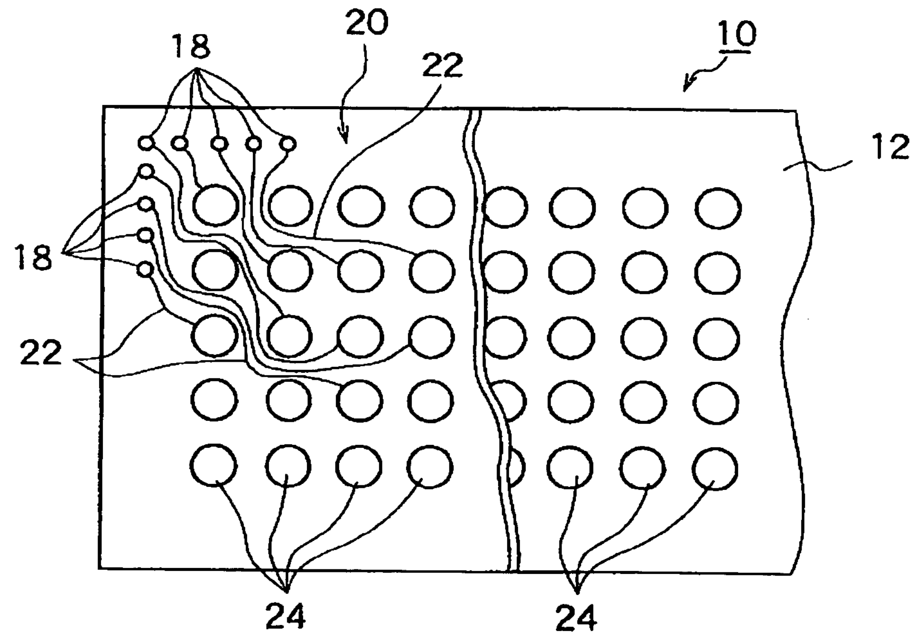

FIG.3

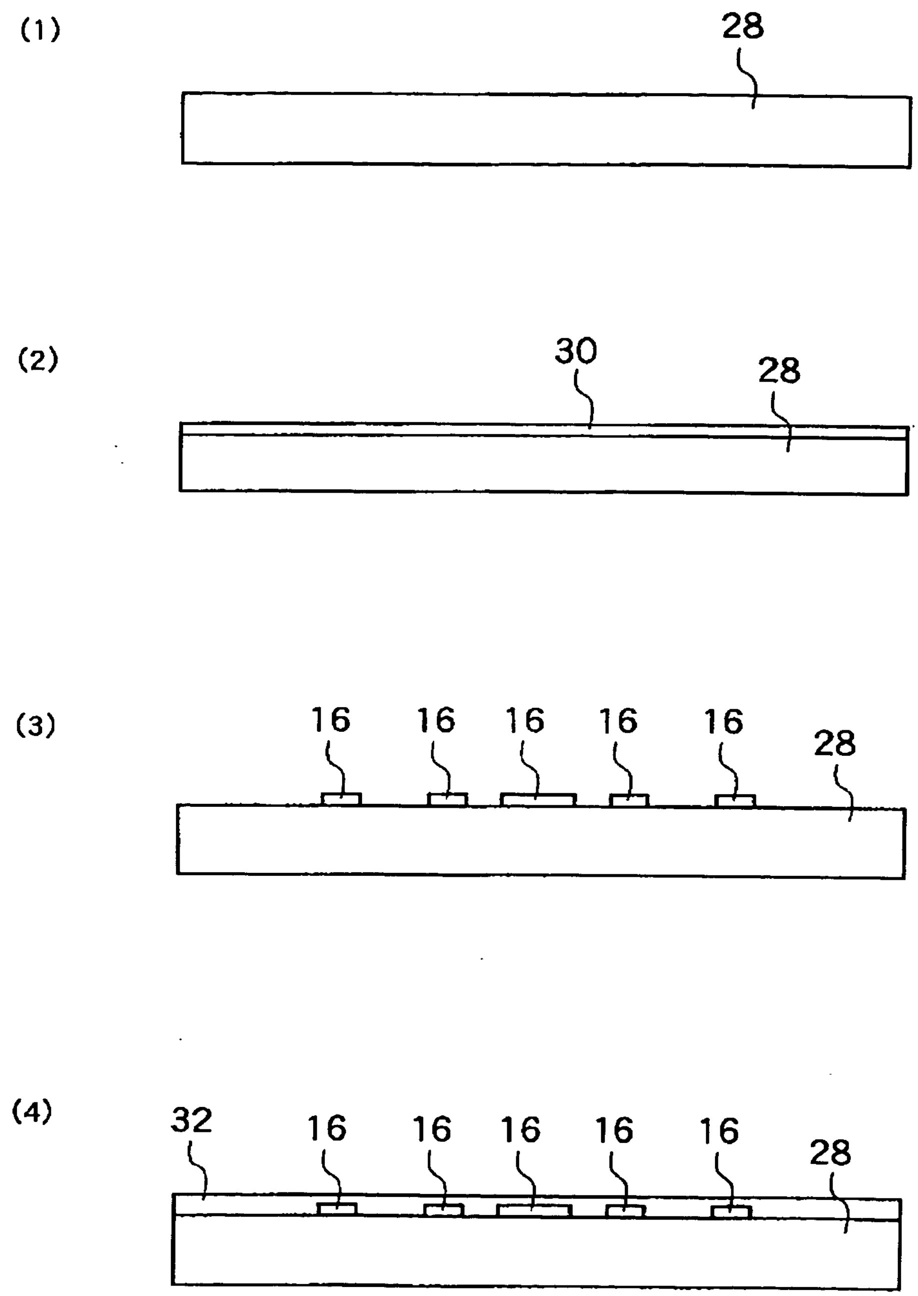

FIG.4

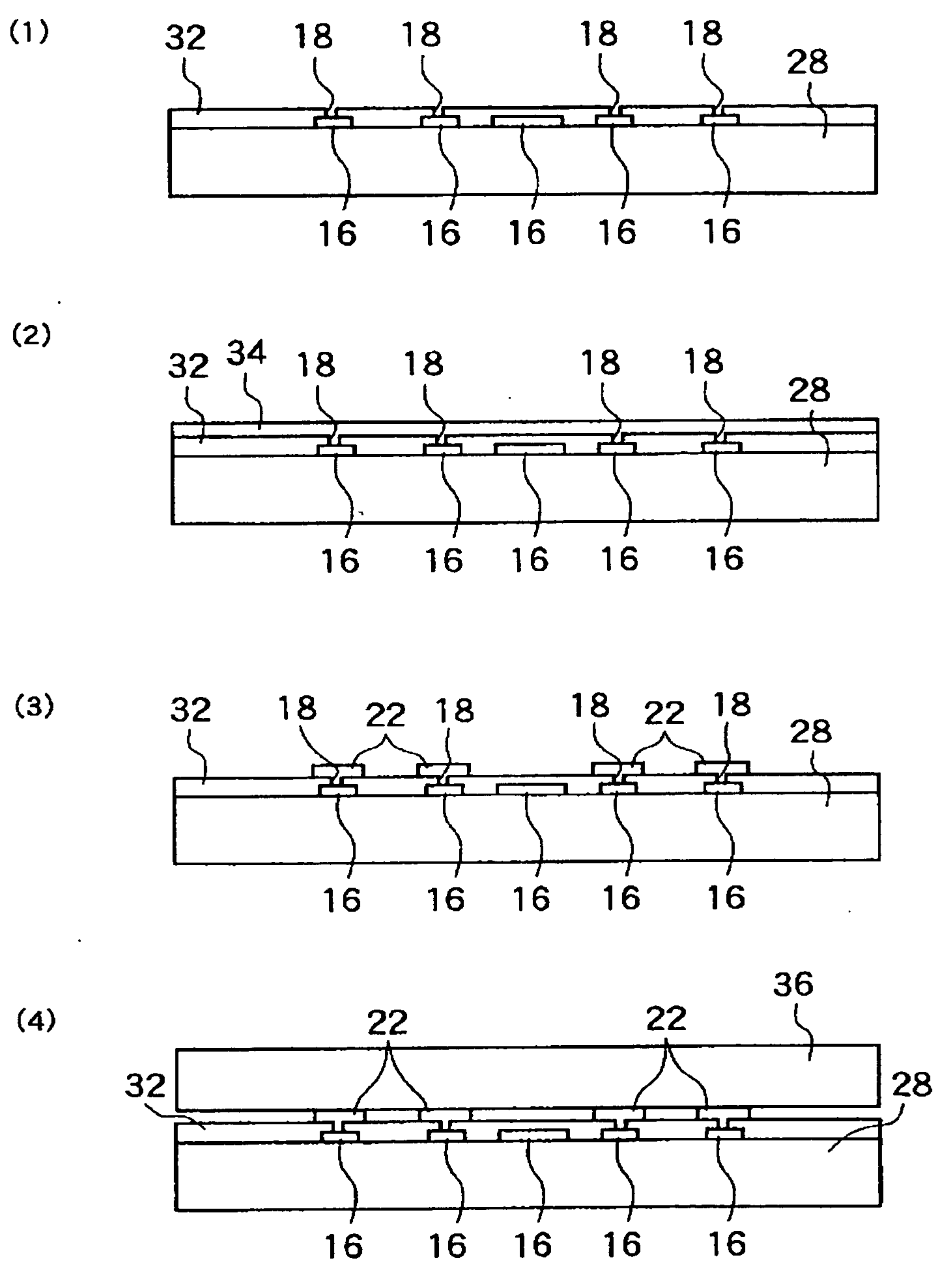

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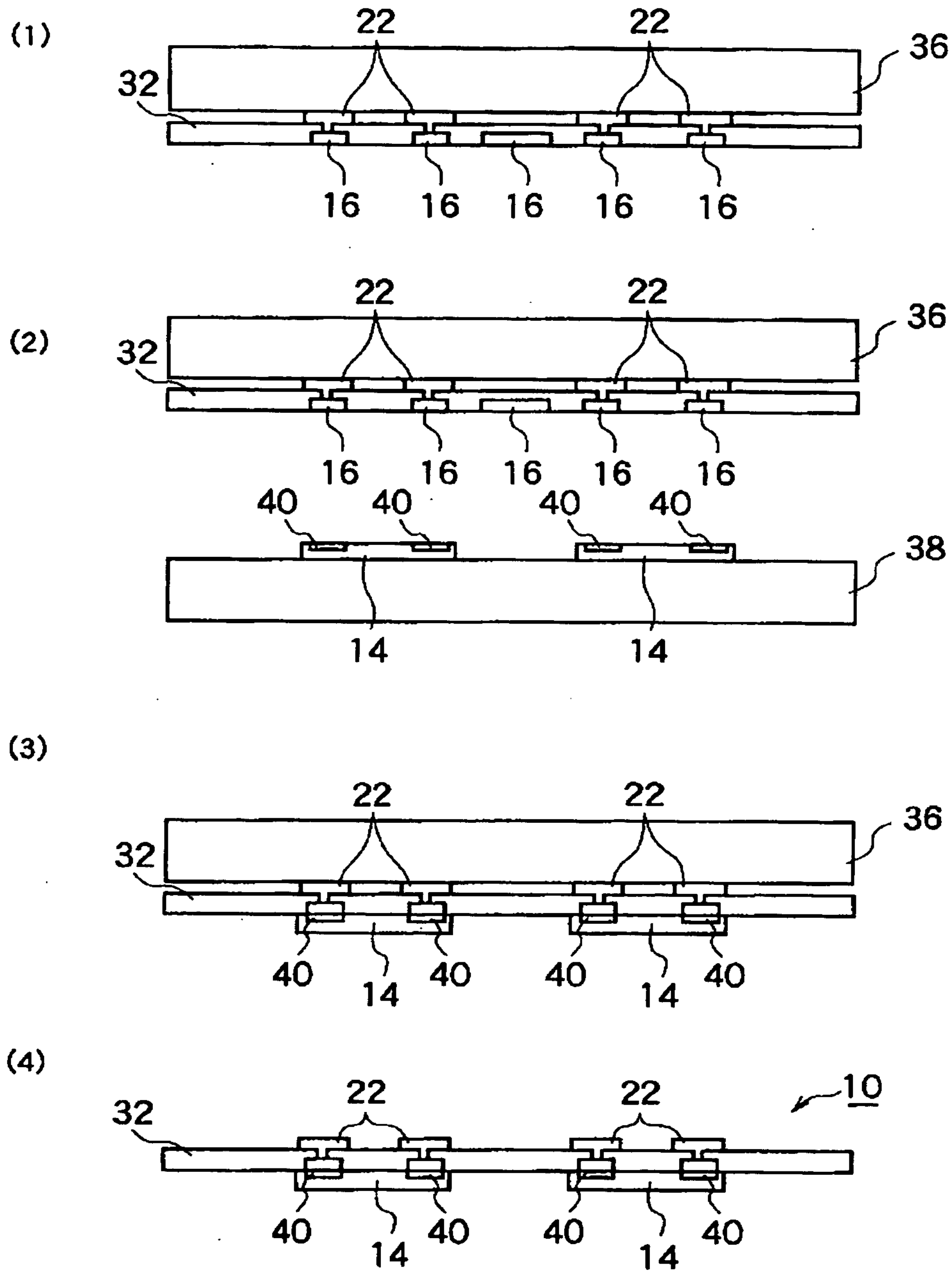
FIG.5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[Name of Document] ABSTRACT

[Abstract]

[Object] To provide a connection board in which the width and pitch of wiring lines can be reduced, a multi-level interconnect structure can be obtained, problems due to radiant heat emitted from a heating tool or the like can be reduced during the mounting of semiconductor chips, and problems such as line breaks caused by external forces can be prevented; a method for manufacturing such a connection board; a semiconductor device; and a method for manufacturing such a semiconductor device.

[Solving Means] First metal lines 16 are formed on a first glass substrate 28. An insulating layer 32 is formed over the first metal lines 16 and second metal lines 22 are then formed on the insulating layer 32. In a connection board 12, deformation is not caused because the first glass substrate 28 is not flexible. Therefore, in a step of forming metal lines, for example, in an exposure sub-step, the glass substrate is not moved in the direction of the depth of field. Thus, precise exposure can be performed and therefore the metal wiring lines having a small width and pitch can be formed.

[Selected Figure] FIG. 1